Summary of Run 2b Silicon Meeting No. 3

Fermilab: July 12, 2000

At this meeting of the Run2b Silicon working group we agreed that we would proceed to study and compare two scenarios in detail. These are indicated below. I also include with asterisks ** the work that is to be done prior to the August meeting and by whom. In addition, there are a number of things that both options have in common. I will list these separately below.

(A) Two Scenarios

(1) Partial SVXII/L00 replacement

For this case we agreed to the following points:

a) The very short shutdown period of 6 months that the lab envisions requires as much pre-construction as possible. We therefore need to prepare new ladder support structures (bulkheads) that would have the new inner layers installed prior to extracting the run2a silicon. The idea would be to make a two-fold support system in which the innermost section is decoupled from the outer one and can be removed separately. It was agreed that in this case, the design of the innermost section (up to a radius of roughly 7-8 cm? could be the same in both replacement scenarios).

** Steve Worm has obtained the costs of the previous bulkheads and their lead times.

b) We believe that the layers that absolutely must be replaced are: L00, L0, and L1. In addition, L2 is marginal as a result of the problems that occur when we attempt to split-bias MICRON silicon. As a result we agreed that we should plan to also replace L2.
** Amit agreed to write up in Tex a brief summary of what is known about L2. This should include a quantitative lifetime estimate.

c) In order to have greater longevity, the replacement layers would need to use single sided silicon, back to back, with integrated cooling.
** Hara has obtained budgetary quotations for silicon for these layers from Hamamatsu

d) We need to understand in as much detail as possible how many L3 and L4 ladders may be damaged or otherwise need replacement when we transfer ladders from SVXII to the new system at SiDet.

** Doug Benjamin agreed to prepare a detailed report on this.

e) We also need a detailed estimate of the time, resources and risks involved in this scenario.
** Doug, Brenna hopefully can prepare a list of work items starting from extraction of the ISL at B0 to its reinstallation. I will work with them to estimate time and resources and evaluate risks.

(2) Complete SVXII/L00 replacement

a) For this option we agreed that the inner most group of silicon layers could be identical to those planned for scenario (1).

b) For the outer layers we agreed that one universal ladder type would be used. The same is true for the inner layers except the L00 replacement. (In both scenarios the geometry of the L00 replacement would not be changed. It is possible that this layer could be double sided or even pixels)

c) For this option, we need to understand in a bit more detail what would be the mechanical support and cooling scheme as well as the cost involved in constructing it.
** Joe I will attempt to prepare something on this if possible. At the moment the engineers who could help understand this are tied up with Run2a work so it may not be possible to do anything very refined.

(B) Common Items

a) Chips:

(i) We have estimates for purchasing more Honeywell SVX3D chips but there was general concern that this is a risky and costly option.

(ii) For a deep sub-micron chip to replace SVX3D we learned:

- LBNL will have a good understanding of the translation possibilities by fall and a submission could be done before year-end if the simulations indicate a successful translation.
- DZero and CDF may be able to use a single chip design provided two obstacles are cleared:
    - an alternate decoding of control signals is provided that matches D0 DAQ specifications.
    - D0 can alter their ladder design (to use alternating strips for instance) such that chips can be placed on hybrids with some spacing to access side-bonds - OR - existing side-bonds can be re-routed to the back of the chip (which looked hard).

b) Hybrids:

For either scenario, we will need new hybrids. We agreed that those for the outer layer would be ceramic, double-sided hybrids as already sketched by Carl Haber. For the inner layers the hybrids would be single-sided and similar to the L00 hybrids.
** Carl agreed to try to come up with an estimate for the cost of hybrids and their lead times.

c) Portcards/optical transmitters

It is likely that old portcards would not work with the SVX4 chips. We could perhaps replace them with newer simpler devices based on rad-hard commercially available components.
** Sergio Zimmerman agreed to prepare some overview of the issues and possible scenarios we could consider. He will also provide some cost information.

d) pixel inner layer(s)

** William Wester agreed to begin more detailed work on the possibility of our using pixels at inner layers. William and the pixel working group will prepare an update on their studies of the following issues:R&D remaining, Material budge & performance, additional DAQ, all costs, schedule, resources (manpower) required, possible additional sources of funding etc.

For the upcoming meeting we will review all new information and begin to refine our plans for a report to the PAC. Hopefully we can begin to write a draft document after this meeting.

Joe Incandela